Specification Update

Server System QSSC-S4R

April 2010

Cloud Computing Business Unit (CCBU),

Quanta Computer Inc.
Revision History

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<thead>
<tr>
<th>Version</th>
<th>Date</th>
<th>Modifications</th>
</tr>
</thead>
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<tr>
<td>1.0</td>
<td>April 2010</td>
<td>Initial release.</td>
</tr>
</tbody>
</table>

Disclaimers

The QSSC-S4R Server System may contain design defects or errors known as errata that may cause the product to deviate from the published specifications. Current characterized errata are documented in this Specification Update.

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Contact your Quanta sales representatives to obtain the latest specifications before placing your product order.

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Preface

This document is an update to the specifications contained in the Server System QSSC-S4R Technical Product Specification. It is intended for hardware system manufacturers and software developers of applications, operating systems, or tools. It will contain specification changes, specification clarifications, errata, and document changes.

Refer to the Multi-Core Intel® Xeon® Processor 7500 Series Specification Update for specification updates processor. Items contained in the Multi-Core Intel® Xeon® Processor 7500 Series Specification Update that either do not apply to the product or have been worked around are noted in this document. Otherwise, it should be assumed that any processor errata for a given stepping are applicable to the Printed Board Assembly (PBA) revisions(s) associated with that stepping.

This documentation communicates the following types of changes:

**Specification Changes** are modifications to the current published specifications for QSSC-S4R server boards. These changes will be incorporated in the next release of the specifications. Specification changes include typos, errors, or omissions from the current published specifications. These changes will be incorporated in the next release of the documents.

**Specification Clarifications** describe a specification in greater detail or further highlight a specification’s impact to a complex design situation. These clarifications will be incorporated in the next release of the documents.

**Errata** are design defects or errors. Errata may cause the server board behavior to deviate from published specifications. Hardware and software designed to be used with any given processor stepping must assume that all errata documented for that processor stepping are present on all devices.
Product Scope

Below are the specific boards, BIOS and components covered by this update.

1. **Product Model: S4R – Server System QSSC-S4R Enterprise SKU**

<table>
<thead>
<tr>
<th>Part #</th>
<th>Main Board Part #</th>
<th>Memory Board Part #</th>
<th>I/O Riser Board Part#</th>
<th>BIOS</th>
<th>Change Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>1S4RZZZ0STI</td>
<td>31S4RMB0000</td>
<td>37S4RRB0000</td>
<td>36S4RIB0000</td>
<td>R0026</td>
<td>Product Launch</td>
</tr>
</tbody>
</table>

2. **Product Model: S4R – Server System QSSC-S4R Value SKU**

<table>
<thead>
<tr>
<th>Part #</th>
<th>Main Board Part #</th>
<th>Memory Board Part #</th>
<th>I/O Riser Board Part#</th>
<th>BIOS</th>
<th>Change Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>1S4RZZZ0STJ</td>
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<td>37S4RRB0000</td>
<td>36S4RIB0000</td>
<td>R0026</td>
<td>Product Launch</td>
</tr>
</tbody>
</table>

3. **Product Model: S4R – Server System QSSC-S4R Board Set – Main Board**

<table>
<thead>
<tr>
<th>Part #</th>
<th>Revision #</th>
<th>BIOS</th>
<th>Change Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31S4RMB0000</td>
<td>D3G</td>
<td>R0026</td>
<td>Product Launch</td>
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4. **Product Model: S4R – QSSC-S4R Board Set – Memory Riser Board**

<table>
<thead>
<tr>
<th>Part #</th>
<th>Revision #</th>
<th>Change Description</th>
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</thead>
<tbody>
<tr>
<td>37S4RRB0000</td>
<td>D3E</td>
<td>Product Launch</td>
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5. **Product Model: S4R – QSSC-S4R Board Set – I/O Riser Board**

<table>
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<tr>
<th>Part #</th>
<th>Revision #</th>
<th>Change Description</th>
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<tbody>
<tr>
<td>36S4RIB0000</td>
<td>E3E</td>
<td>Product Launch</td>
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</table>


<table>
<thead>
<tr>
<th>Part #</th>
<th>Revision #</th>
<th>Change Description</th>
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<tr>
<td>AD035460000</td>
<td>D</td>
<td>Product Launch</td>
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</table>
7. **Product Model: S4R – QSSC-S4R Board Set - Hot Swap Backplane**

<table>
<thead>
<tr>
<th>Part #</th>
<th>Revision #</th>
<th>Change Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>35S4RHB0000</td>
<td>E3C</td>
<td>Product Launch</td>
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8. **Product Model: S4R – QSSC-S4R Board Set - Front Panel Fan Board**

<table>
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<th>Part #</th>
<th>Revision #</th>
<th>Change Description</th>
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<td>34S4RFB0010</td>
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<td>39S4RPA0000</td>
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10. **Product Model: S4R – QSSC-S4R Board Set - Power Distribution Board**

<table>
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<tr>
<th>Part #</th>
<th>Revision #</th>
<th>Change Description</th>
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<tbody>
<tr>
<td>AFPDB000013</td>
<td>1A-03</td>
<td>Product Launch</td>
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Summary Tables of Changes

The following tables indicate the errata and the document changes that apply to the server system QSSC-S4R. Quanta intends to fix some of the errata in a future stepping of components, and to account for the other outstanding issues through documentation or specification changes as noted. The tables use the following notations:

- **Doc:** Quanta intends to update the appropriate documentation in a future revision.
- **Fix:** Quanta intends to fix this erratum in the future.
- **Fixed:** This erratum has been fixed.
- **No Fix:** There are no plans to fix this erratum.
- **Shaded:** This erratum is either new or has been modified from the previous specification update.

Table 1. Errata Summary

<table>
<thead>
<tr>
<th>No.</th>
<th>Plans</th>
<th>Description of Errata</th>
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<td>Fix</td>
<td>BIOS Default to DDR3 DIMM single refresh instead of the desired double refresh.</td>
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<td>Fix</td>
<td>ESX 4.0 U1 is reporting MPC table too large error message</td>
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<td>Fixed in BIOS 26</td>
<td>When SMT is enabled, processor domain, p-state and c-state does not work properly</td>
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<td></td>
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<td>under both Windows 2008 and Windows 7 Operating Systems.</td>
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<td>5.</td>
<td>Fix</td>
<td>Multiple Hotplug test for memory riser with MBIST DIMM fail &amp; status</td>
</tr>
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<td>6.</td>
<td>Fix</td>
<td>Active Processor Cores setting incorrect</td>
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<td>7.</td>
<td>Fix</td>
<td>No error messages after inserting an MBIST failed DIMM after system boot. Memory</td>
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<tr>
<td></td>
<td></td>
<td>Error detection / BIST fails</td>
</tr>
<tr>
<td>8.</td>
<td>No Fix</td>
<td>BIOS hidden Setup options should not be seen in AMIBCP utility</td>
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<tr>
<td></td>
<td></td>
<td>error event</td>
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<td>11.</td>
<td>Fix</td>
<td>The system will reset and log CATERR after hot-adding failed memory under DIMM</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Sparing / [2 Way] Interleave mode</td>
</tr>
<tr>
<td>12.</td>
<td>Fix</td>
<td>The system does not boot to USB key when hard reset is performed.</td>
</tr>
<tr>
<td>13.</td>
<td>No Fix</td>
<td>EFI Self Certification Test failures</td>
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<td>System fails to boot up and lights CATERR led under Mixed Stepping processor &gt; 1</td>
</tr>
<tr>
<td></td>
<td></td>
<td>stepping apart.</td>
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<td>15.</td>
<td>Fixed in BIOS 25</td>
<td>No error beep code sounded during Channel Training Error</td>
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<td>---</td>
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<td>16.</td>
<td>Fixed in BIOS 26</td>
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<tr>
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<tr>
<td>28.</td>
<td>No Fix – DOC#043 02010</td>
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<td>OFU build -14 : HSC update &amp; FW update fails on Linux (RHEL 5.4/SLES 11) OSes with the OPEN IPMI driver fail-over issue</td>
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<td>4.</td>
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</tbody>
</table>

Following are in-depth descriptions of each erratum / documentation change indicated in the tables above. The errata and documentation change numbers below correspond to the numbers in the tables.
## Errata

1. **BIOS Default to DDR3 DIMM single refresh instead of the desired double refresh**

   **Problem**
   EmeraldRidge BIOS does not currently enable Double Refresh. Quad Rank DIMMs need Double Refresh to prevent frequent throttling.

   **Implication**
   Under maximum ambient conditions the system may throttle more than 50% of the time. Under typical ambient conditions the system may throttle approximately 10% of the time.

   **Workaround**
   None

   **Status**
   Fix

2. **ESX 4.0 U1 is reporting MPC table too large error message**

   **Problem**
   ESX 4.0 U1 shows error message: 
   
   TSC : 2771848 cpu0:0) MPS: 732: 
   MPC table too large, its size (61440) is > than max (8192). Skipping table! 

   MPC table is larger than the maximum size.

   **Implication**
   Can not boot into ESX 4.0 U1.

   **Workaround**
   None

   **Status**
   Fix

3. **No WHEA logs for “Uncorrectable hardware error” after MBE under DIMM sparing mode**

   **Problem**
   When an uncorrectable error occurs on a memory, WHEA should have “Uncorrectable hardware Error”.

   **Implication**
   The user cannot understand what happened to the system via OS (only with Windows* 2008 Server) event viewer. There will be BMC SEL log for this error.

   **Workaround**
   None

   **Status**
   Fix
4. When SMT is enabled, processor domain, P-state and C-state does not work properly under both Windows 2008 and Windows 7 Operating Systems

Problem When SMT is enabled, all 64 processors in Windows Device manager has yellow mark. Messages from processor’s properties window indicated that processor driver could not be started because it was waiting on some other devices to start first.

Implication The user will observe “Yellow Bang Marks” for processors in Device Manager. The user will be confused with the “Yellow Bang Marks” of processors in Device Manager.

Workaround None

Status Fixed in BIOS R0026 and D0 CPU

5. Memory Hot-plug test for memory riser with MBIST DIMM fail & Status

Problem The user will not be notified if there is any MBIST failed DIMMs on the Memory Board during the Memory Hotplug process. This issue occurs only when the Memory board is hot plugged with an MBIST failed DIMM.

Implication The user will not be notified by the BIOS if the MBIST failures that occur on any of the DIMMs on Memory board during memory Hot Plug process.

Workaround None

Status Fix

6. Active Processor Cores setting incorrect

Problem In 4 or 6 core processors, the cores enabled during manufacturing are not symmetric. Therefore, the number of cores enabled in the processors are not uniform when applying “active core mask” directly. The issue happens only with 4 or 6 core processors.

Implication The number of cores enabled will be not be consistent when “active core mask” is set. This option is used to reduce the performance, thereby saving power. This issue is low risk as few customers will use this option to reduce performance.

Workaround None

Status Fix
7. No error messages after inserting an MBIST failed DIMM after system boot. Memory Error detection / BIST fails

Problem: Errors are not reported in the Error Manager for the MBIST failed DIMM on Memory Board. This issue occurs only when there is MBIST failed DIMM in the system.

Implication: The customer will not be notified by Platform BIOS if there is any MBIST failed DIMM in the system, BIOS will show these failed DIMMs as disabled in Error Manager/setup.

Workaround: None

Status: Fix

8. BIOS hidden Setup options should not be seen in AMIBCP utility

Problem: The AMIBCP utility should not show/allow user to change the hidden setup options.

Implication: The AMIBCP is a utility used to change BIOS default settings by updating BIOS Capsule. AMIBCP is an utility used to change BIOS default settings by updating BIOS Capsule file. The utility currently shows all hidden setup options, thus enabling the user to change them. Customers should not have the ability to change hidden setup options.

Workaround: None

Status: No Fix

9. QPI Error injection test fails under errors on both Data lanes and CLOCK lanes.

Problem: QPI Error injection failure for both Data lanes and Clock Lanes. After injecting the errors, the SEL logs a QPI fatal error with the wrong socket ID. There is no WHEA event and the system does not hang or reboot.

Implication: The customer is not notified of QPI errors, as there is no SEL event, WHEA event, or system hang/reboot.

Workaround: None

Status: Fixed in BIOS R0026 and D0 CPU
10. **Hot replace memory riser with BIST failed DIMM under Intra-Mirror mode reports wrong error event.**

**Problem**  The user will not be notified if there is any MBIST failed DIMMs on the Memory Board during Memory Hotplug process. The issue only occurs when the Memory board is hot plugged with MBIST failed DIMM.

**Implication**  The customer will not be notified by Platform BIOS if the MBIST failures that occur on any of the DIMMs on Memory board during memory Hot Plug process.

**Workaround**  None

**Status**  Fix

11. **The system will reset and log CATERR after hot-adding failed memory under DIMM Sparing / [2 Way] Interleave mode.**

**Problem**  Hot-adding a memory board with failed memory will cause a system reset and log CATERR DIMM Sparing / [2 Way] Interleave mode. The Hot-add operation should gracefully fail by powering off the memory board with a SEL event sensor number 20h.

**Implication**  When a riser with bad population is hot added, customers will expect the BIOS to reject the hot add and turn off the riser. The system will reset with a CATERR.

**Workaround**  None

**Status**  Fix

12. **The system does not boot to USB key when hard reset is performed.**

**Problem**  On some models of USB Keys, when a system hard reset cycle is performed, the USB key does not get detected.

**Implication**  The customer may see USB key detection failure very rarely, however reinserting the key (without rebooting the system) will detect it.

**Workaround**  Reinsert the USB key without rebooting the system.

**Status**  Fix
13. **EFI Self Certification Test failures**

**Problem**
When the UEFI Self Test compliance test tool 2.1 is executed, there are several failed items.

**Implication**
The platform BIOS is UEFI 2.0 compliant, however, the tool is UEFI 2.1 compliant. There is no customer impact when using UEFI test tool 2.0.

**Workaround**
Use UEFI test tool 2.0 for this platform.

**Status**
No fix.

14. **System fails to boot up and lights CATERR led under Mixed Stepping processor > 1 stepping apart.**

**Problem**
After installing a 1.86GHz, D0, Q3X9 in CPU socket 1 and 2.13GHz, B1, Q3CB in CPU socket 2, the system fails to boot up. The CATERR led lights.

**Implication**
Customers can not use D0/B0 processor combination. If used, system will display CATERR.

**Workaround**
Use combination of newer stepping processors (>C0), for example, C0/D0 processor combination.

**Status**
No Fix.

15. **No error beep code sounded during Channel Training Error**

**Problem**
No error beep code sounded during Channel Training Errors. BIOS should beep when there are failed DIMMs in the system.

**Implication**
When system power is lost the iBBU can take up to 400us to sense the drop in 1.8V and apply power to the RAID DIMM. A system with 1.8V drawn from a 3.3V power regulator would not have this delay. In lab testing this short delay put the RAID DIMM temporarily outside the memory vendors’ specification. This could potentially lead to data stored in cache, and not yet written to disk, to be lost. If data integrity is compromised a message will be displayed on the next boot: “Controller cache discarded due to memory/battery problems.

**Workaround**
Customers will not hear beep codes even though there is a channel training error on few DIMMs.

**Status**
Fix
16. **Cannot press <CTRL-I> to enter SW RAID OPROM from remote system HyperTerminal through console redirection**

**Problem** Configuration of SoftWare RAID option from remote console such as HyperTerminal/SOL fails when using <CTRL-I> to enter SW RAID OPROM from remote system hyperterminal.

**Implication** Customer will not be able to configure SWRAID from remote console when using <CTRL-I> as per the industry specification. m Event Log.

**Workaround** Press ESC+^+B+I to configure SWRAID from remote console.

**Status** Fix

17. **BMC is not getting the Platform Event Message for Permanent Memory Power good failures via SMS**

**Problem** For any failed memory riser in the system, the BIOS should disable the memory riser and inform the BMC of the failed riser. BIOS currently disables the riser but fails to notify the BMC.

**Implication** When BIOS finds a permanently failed riser on EmeraldRidge system, it disables the risers and continues to boot with the remaining risers. However, BIOS does not notify the disabled riser state. System Status and SEL will not indicate the failure.

**Workaround** None

**Status** Fix – plan to fix in BIOS R0027

18. **System fails to boot and will emit 3 error beep code after BIOS update.**

**Problem** After updating R0023 to later BIOS (R0024, R0025, R0026), an EFI Shell “reset” command will cause a Memory Detection Failure. The system would hang during POST. The BIOS will emit 3 error beep codes, indicating memory detection has failed.

**Implication** The system will not boot to the new BIOS and will emit 3 error beep codes. The user must DC or AC power cycle the system to boot.

**Workaround** After updating the BIOS to any later BIOS, an AC or DC power cycle is required only on the first boot to the later BIOS. An AC or DC power cycle is not required for every boot after the initial boot of the new BIOS. When updating the BIOS remotely, DC cycling of the system can be accomplished by using one of the IPMI Chassis Control Commands as defined in the Intel®
Command Line Interface User Guide. Please refer to the guide for the appropriate command line options.

Status Fix

19. Memory devices not shown correctly in OS Device-Manager when 8-way interleaving is selected with NUMA disabled.

Problem When NUMA is disabled, with no interleaving, there will be 8 Memory modules shown in Device Manager. When NUMA is disabled with 2-Way interleave, there will be 4 memory modules in Device Manager. When NUMA is disabled with 4-Way interleave enabled, there will be 2 memory modules in Device Manager. However, with NUMA disabled with 8-Way interleave enabled, memory modules are not displayed (reason unknown).

Implication The relationship between physical memory risers and memory modules in device manager is somewhat confusing. There is no functionality impact in various interleave/NUMA modes. It is the device manager information that is not getting displayed as expected.

Workaround None

Status Fix

20. Injecting SBE fails with Intra-Socket Mirrored Mode

Problem When Single Bit correctable Errors are injected on Master in Mirror mode, they are reported as Uncorrectable errors and Mirror Fail over occurs

Implication Thr SDDC engine can correct up to 4 single Bit errors. Disabling SDDC in Mirror Mode, will result treating 2-Bit correctable errors as uncorrectable errors. There is no significant customer impact. However, redundancy will be lost whenever there is greater than a 2 Bit error.

Workaround None

Status Fixed in BIOS R0026
21. **BMC - HSC communication fails after continuous chassis control hard reset cycles**

- **Problem**: HSC communication fails after continuous chassis control hard reset cycles and running ipmitool sensors cmd
- **Implication**: The user will not be able to communicate to the HSC after hard reset test and sensor scanning in parallel.
- **Workaround**: Issue a cold reset command to BMC by KCS or LAN interfaces
- **Status**: Resolved in BMC 17

22. **RMM3 KVM - Mouse does not work in the Big Laurel SAS option ROM**

- **Problem**: Mouse does not work in Big Laurel SAS Option ROM
- **Implication**: Must configure RAID configurations with keyboard input.
- **Workaround**: None
- **Status**: Fix

23. **BMC reporting Power Supply OTP events in SEL when system powers-on at elevated ambient temperature**

- **Problem**: BMC reporting Power Supply OTP events in SEL when system powers-on at elevated ambient temperature
- **Implication**: Customers might see a SEL entry for PS temperature sensors crossing upper non-critical during power on. No impact to system functionality.
- **Workaround**: None
- **Status**: Fix
24. All system fan lower (non)critical asserted events logged during AC power cycle test

Problem: All system fan lower (non)critical asserted events logged during AC power cycle test. The frequency at which these events occur is low, occurring at the rate of ~7 out of 200 cycles.

Implication: Customer will see fan lower critical events with lower RPM in SEL Log during AC cycle test. This issue is not seen during regular operations when the system is running.

Workaround: None

Status: Fix

25. Issue updating complete SW stack via PXE boot using WinPE x64

Problem: ME and BMC FW update fails via PXE boot on WinPE X64.

Implication: Mass deployment Via PXE boot on WinPE x64 will not work

Workaround: EFI and Windows standalone utilities (OFU) work.

Status: Fix

26. Fwpiaupd 5.0.1 Build 2 _Winpe_3.0/2.0 on 32 bit OS: HSC update fails with Microsoft-IPMI driver

Problem: HSC FW update failed using MS IPMI driver on WinPE 3.0/WinPE 2.0 32 Bit version.

Implication: Will notice issue only with MS IPMI driver on Windows 2003 and Windows 2008. Intel drivers can be used after disabling Microsoft drivers.

Workaround: Intel/Open IPMI Driver needs to be installed separately after disabling MS IPMI driver.

Status: Fix
27. **Cold Redundancy (CR) is not completely functional**

**Problem**
Cold Redundancy (CR) does not provide complete power supply redundancy in all PS operating and failure conditions. Cold redundancy is completely functional only when the system is started with 4 PS installed and at least 2 PS are active; otherwise the system is operating in warm redundancy.

**Implication**
When in CR mode, if a hard failure occurs on the single active PS (when only one PS is active), the system PWOK may get de-asserted. This de-assertion will cause the system to reset. The root cause for this issue is excessive fault signal delay in the PS and power distribution board (PDB) micro-controllers. Risk of system reset/shutdown only occurs if system is operating in Cold Redundancy, and the single active PS experiences a hard failure.

**Workaround**
Systems shipped at SRA will have this feature disabled via the CR jumper on the PDB to avoid the risk described above.

**Status**
Fix – plan to add Cold Redundancy (CR) feature back with 01F PS/PDB

28. **Memory controller SMI lane fail-over issue**

**Problem**
SMI lane fail-over events may be randomly logged in the SEL (system event log) during manufacturing testing and/or after initial installation of the memory risers.

**Implication**
Customers may see SMI Lane Fail-over events in the system event (SEL) log after the initial installation of memory risers. There is no impact to system functionality, reliability, or performance.

**Workaround**
Re-seating memory riser clears this problem.

**Status**
No Fix – this is a known behavior of QSSC-S4R. Refer to DOC#04302010 for more detail.

29. **OFU build -14 : HSC update & FW update fails on Linux (RHEL 5.4/SLES 11) OSes with the OPEN IPMI driver fail-over issue**

**Problem**
The platform BMC & HSC FW update fails with Linux open IPMI driver in GUI mode and intermittently in console mode.

**Implication**
Customers will see this issue when using the Open IPMI driver.
Workaround  The Intel IPMI Driver can be used after disabling Linux Open IPMI Drivers. The Intel/Open IPMI Driver needs to be installed separately.

Status  Fix

30.  OFU build 14: BMC update & FRUSDR update fails on Windows 2K3 R2 SP2 OS with MSIPMI driver

Problem  The HSC FW update failed using MS IPMI driver on WinPE 3.0/WinPE 2.0 32 Bit version.

Implication  Customers will see this issue when issue only with the MS IPMI driver on Windows 2003 R2 SP2 32 bit.

Workaround  The Intel IPMI Driver can be used after disabling the MS IPMI drivers. The Intel Driver needs to be installed separately.

Status  Fix

31.  WHEA Memory errors logged do but not contain correct detailed info

Problem  W2K8R2 x64, correctable ECC memory error in MEMR1 1B will log WHEA events properly but details do not contain correct information.

Implication  WHEA logs will be generated but some information will be missing from OS log.

Workaround  None.

Status  Fix

32.  No Solaris support for Intel(R) 82576NS network devices

Problem  Intel(R) 82576NS onboard network devices can’t be detected under Solaris 10 update 7 Build 8 x86. Solaris does not have embedded driver support.
Implication No Solaris support for Intel(R) 82576NS onboard network device until Solaris 10 U9.

Workaround Use release patch for U8 when available

Status Fix

33. MS Performance Monitor (Perfmon) shows Processors not running at less than maximum rated frequency when Turbo mode enabled.

Problem When stressing the system with Turbo mode enabled, Performance Monitor (Perf Mon) does not display the correct processor frequency.

Implication The customer will not see the correct processor frequency while in Turbo mode when using Perfmon.

Workaround None

Status Fix

34. Cannot install Windows 2008 SP2 64-Bit under SATA SW RAID mode.

Problem W2K8 SP2 64bit failure to install to SATA SW RAID. The system stops installation during the roll bar. The failure is specific to Matrix SW RAID with 64 CPU threads. Able to workaround failure by limiting OS to 63 threads.

Implication No SW RAID support for W2K8 with max CPU configuration.

Workaround Able to workaround failure by limiting OS to 63 threads.

Status Fix

35. Hot replacing PCI-e cards on slot 1, 2, 6, 7 fails under W2K8 R2 x64

Problem Current PCI Express ACPI code does not implement a handler to deal with Presence Detect Enable status change, which may cause the system failing to initiate the slot with the replacement when hot-replacing a PCI-e card on slot 1,
2, 6 or 7 shortly after the previous hot plugging (adding or removal) step is performed.

Implication  Immediate hot replacing action following the hot plugging (adding or removal) step will fail to initiate the slot with the replacement PCI-e card.

Workaround  After hot plugging (adding or removal), wait for a few more minutes before performing the follow-on step to hot swap.

Status  Fix – will fix in BIOS R0027

36. Memory Attention LED on Memory Riser is not functional

Problem  Current memory hot plug spec does not support the ATTN LED behavior and BIOS has no hooks to support the same, as described in the memory riser label.

Implication  The customer will not see this ATTN LED lit during hot add or hot swap operations of memory riser.

Workaround  None – the Power LED suffices the hot plug event indications. The current status is to have all hot plug events indicated through the Power LEDs.

Status  Fix – will fix in BIOS R0027
Documentation Changes

1. Hot swappable fan is not supported in non-redundant fan configurations.

Problem
If a fan is hot-swapped in a non-redundant fan configuration, the system treats it as a fan failure. This is normal operation. The current 1.0 revision of the EPS is incorrect.

Status
The BMC EPS will be modified in version 1.1 to reflect the following:

14.1.1

Server Chassis Support for QSSC-S4R
The following Server Chassis are used with Server Boards with the Intel® Chipset.

Table 77. Server Chassis Support

<table>
<thead>
<tr>
<th>Server Chassis</th>
<th>Chassis-specific Server Management Features</th>
<th>Chassis-dependent Sensors Managed by BMC</th>
</tr>
</thead>
<tbody>
<tr>
<td>ROW Entry SKU</td>
<td>▪ Non-redundant cooling:</td>
<td>▪ Four fan tachometer sensors</td>
</tr>
<tr>
<td>Non-Redundant Cooling</td>
<td>▪ Four chassis fans which are not hot swappable.</td>
<td>▪ One front panel temperature sensor</td>
</tr>
<tr>
<td></td>
<td></td>
<td>▪ One power unit redundancy sensor</td>
</tr>
<tr>
<td>ROW Enterprise SKU</td>
<td>▪ Redundant cooling: Eight chassis fans which are hot swappable, technically it is 7+1 fan cooling solution in which can tolerate only one fan failing</td>
<td>▪ Eight fan tachometer sensors</td>
</tr>
<tr>
<td>Redundant Cooling</td>
<td></td>
<td>▪ One fan unit redundancy sensor</td>
</tr>
<tr>
<td></td>
<td></td>
<td>▪ One front panel temperature sensor</td>
</tr>
<tr>
<td></td>
<td></td>
<td>▪ One power unit redundancy sensor</td>
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</table>